

## Features

- Parallel Inputs and Outputs
- 32 x 9 FIFO
- Stand Alone
- Data Rates up to 5.0MHz
- Independent Reading and Writing
- Half-Full FLAG
- Last Word Retention
- TTL – Compatible Tri-state Outputs
- Input and Output Ready Signals
- Master Reset
- Single +5V Supply

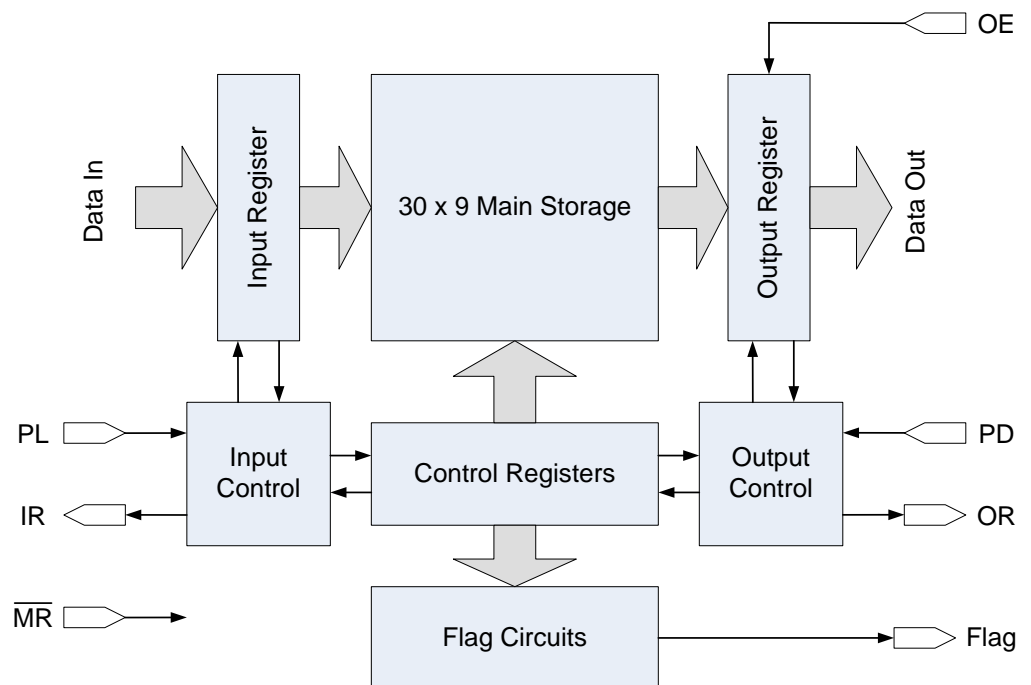
## Description

The **FS2813HS** is a form, fit, function replacement for the MJ2813, a 32-word by 9-bit first-in first-out (FIFO) memory. The device has completely independent read and write controls and three state outputs controlled by an output enable pin (OE). Data on the data inputs (D<sub>0</sub> – D<sub>8</sub>) is written into the memory by a pulse on load (PL). The data word automatically ripples through the memory until it reaches the output or another data word.

Data is read from the memory by applying a shift out pulse on PD. This dumps the word on the outputs (Q<sub>0</sub> – Q<sub>8</sub>) and the next word in the buffer moves to the output. An output ready signal (OR) indicates that data is available at the output and also provides a memory empty signal. An input ready signal (IR) indicates that the device is ready to accept data and also provides a memory full signal.

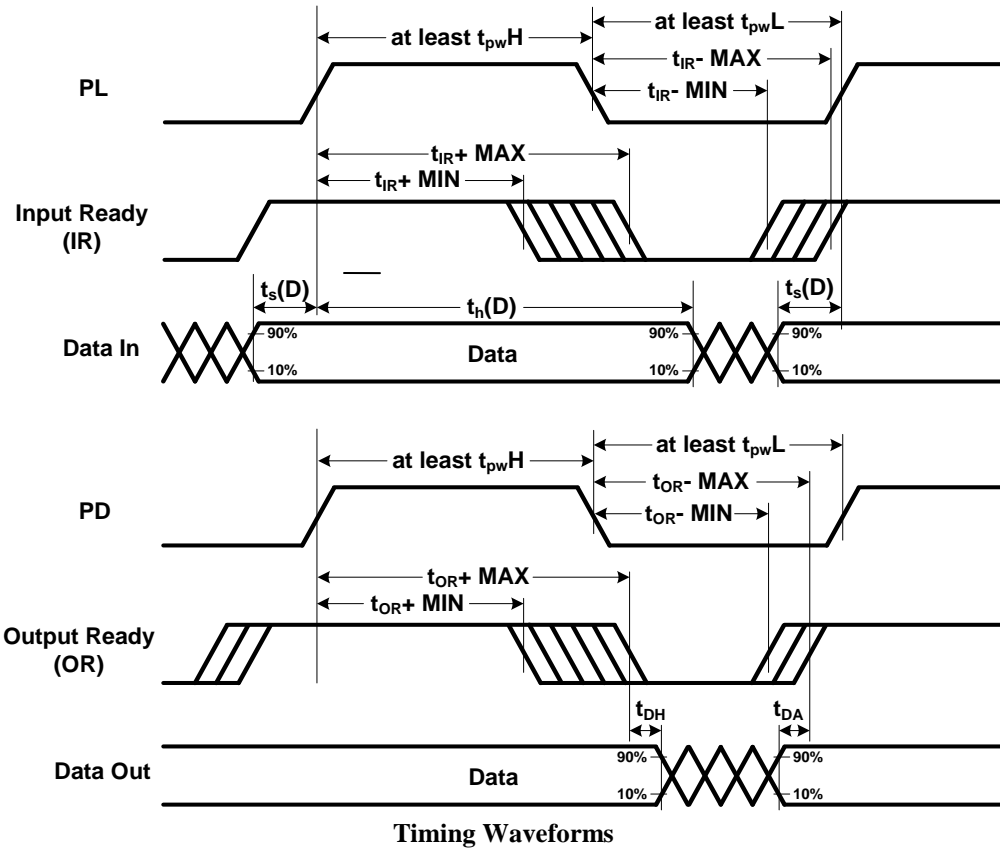
The FS2813HS has master reset inputs which initialise the FIFO control logic and clear all data from the device (reset to all lows). A FLAG signal goes high when the memory is half full.

The timing and function of the four control signals PL, IR, PD and OR are designed so that two FIFOs can be placed end-to-end, with OR of the first driving PL of the second and IR of the second driving PD of the first. With this simple interconnection, strings of FIFOs can control each other reliably to make a FIFO array any number of words deep. Cascadability is only guaranteed up to 3MHz data range.

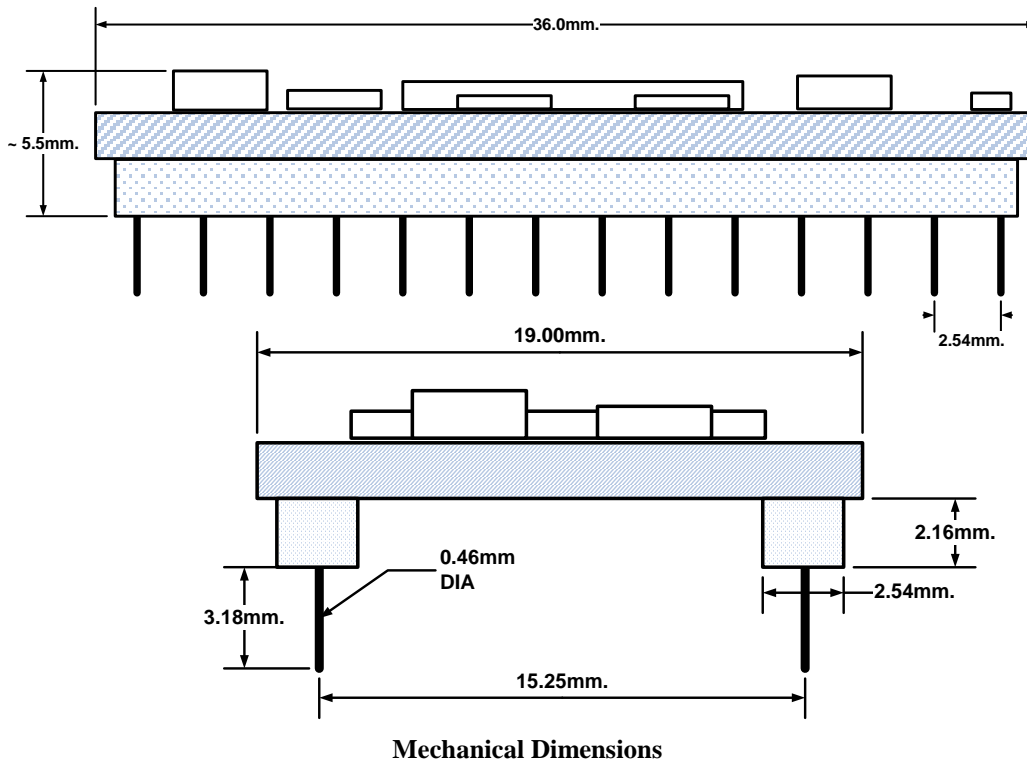


**Functional Diagram**

## Timing Diagram



## Dimensional Package Outline



## Absolute Maximum Ratings

Symbol	Description	Industrial	Unit
Tstg	Storage Temperature	-65 to +150	°C
	Temperature (ambient) under bias	-55 to +125	°C
	Voltage on any pin to ground (OV)	-0.3 to +9	V
Vin	DC input voltage	-0.3 to +6	V

## Operating Range

Type number	Ambient Temperature	Vcc	Ground
FS2813HS	0°C to +70°C	5.0V ± 5%	0V

## DC Electrical Characteristics

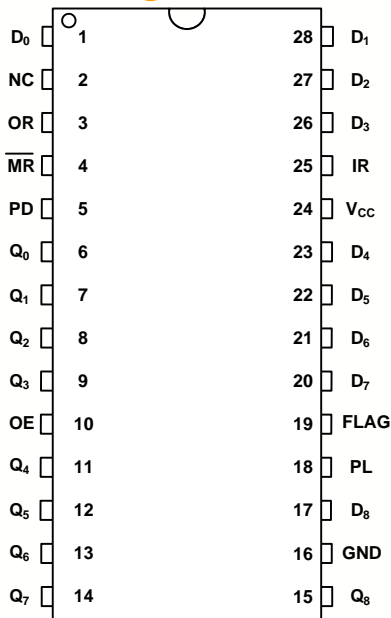
Symbol	Parameter	Value			Unit	Conditions
		Min.	Typ.	Max.		
VOH	Output high voltage	2.4			V	IOH = -0.3mA
VOL	Output low voltage			0.4	V	IOL = 1.6mA
VIH	Input high voltage	2.5			V	
VIL	Input low voltage			0.8	V	
VIL	Input leakage current			10	µA	VIN = 0V
VIH	Input high current			10	µA	VIN = 5.25V
ICC	VCC current		70	114	mA	Tamb = 0°C to +70°C
			70	120	mA	Tamb = -55°C to +125°C

## AC Electrical Characteristics Industrial

Symbol	Parameter	MJ2813HS			Unit	Conditions
		Min	Typ.	Max		
fp	Maximum parallel load or dump frequency	4.1	5	*	MHz	
tIR	Delay, PL or SL high to IR inactive		180	200	ns	
tIR	Delay, PL or SL low to IR active		200	350	ns	
tpwH(P)	Minimum PL or PD high time			8	ns	
tpwL(P)	Minimum PL or PD low time			100	ns	
th(D)	Data hold time			200	ns	
ts(D)	Data set-up time			0	ns	to PL
tOR +	Delay, PD high to OR low		125	240	ns	OE high
tOR -	Delay, PD low to OR high		200	400	ns	DE high
tPT	Ripple through time		1	2.5	µs	FIFO empty
tDH	Delay, PD low to data out changing			240	ns	
tDA	Delay, data out to OR high		0		ns	PD = high
tMRO	Minimum reset pulse width			290	ns	
tDO	Delay, OE low to output off			250	ns	
tEO	Delay, OE high to output active			250	ns	
tDF	Delay from PL low to FLAG high or PD low to FLAG low		700	1000	ns	
CI	Input Capacitance			7	pF	

\*Cascadability only guaranteed to 3MHz

## Pin Configuration



## Pin Descriptions

Pin Name	Dir	Description
<b>Input port</b>		
D[8:0]	In	Data Inputs, 9bits
IR	Out	Input Ready flag. A logic high ('1') indicates device ready and able to accept new input data. Also acts as a memory full indication flag.
PL	In	Parallel Load. Loads byte of data present on all D[8:0] pins into FIFO (parallel transfer).
<b>Output port</b>		
Q[8:0]	Out	Data Outputs, 9bits
OE	In	Output Enable. Q[8:0] output pins are tri-stated when OE inactive (low).
OR	Out	Output Ready. Flag indicating when valid data is present on output pins Q[8:0]
PD	In	Parallel Dump. Transfers next data byte from FIFO memory onto output pins Q[8:0] (parallel transfer)
<b>Other</b>		
MR*	In	Master Reset ( <b>Active Low</b> ). A low pulse resets the device.
FLAG	Out	FIFO Half-full indication. Flag set when FIFO approximately half full.
GND	Out	Ground
VCC	In	Power
NC	-	No connect

**Table 1 Pin Descriptions**

Note: unless otherwise indicated (by \*), all controls/flags are active high operation.

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